



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/785,587	02/24/2004	Masao Noro	308455 H8072US	3201

7590 03/21/2008
Pillsbury Winthrop LLP
Intellectual Property Group
Suite 2800
725 South Figueroa Street
Los Angeles, CA 90017-5406

EXAMINER

PAUL, DISLER

ART UNIT	PAPER NUMBER
----------	--------------

2615

MAIL DATE	DELIVERY MODE
-----------	---------------

03/21/2008

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No. 10/785,587	Applicant(s) NORO ET AL.	
	Examiner DISLER PAUL	Art Unit 2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. ____. |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>2/24/04;8/15/07;2/15/08</u> . | 6) <input type="checkbox"/> Other: ____. |

DETAILED ACTION

Response to Arguments

In regard to the applicant's argument/amended claims wherein the disclose feature of having the "predetermined delay to a first drive signal", notice, such limitation is indeed disclosed by Johnson wherein there is disclosed of a lag delay between the driving signals (fig.4, col.3 line 5-12), thus such limitation is anticipated by Johnson.

Response to Amendment

The examiner has further considered the amended/added new claims in view of Johnson (US 6,181,796 B1) and Chuang (US 6,748,096 B2).

1. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3,6 are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson (US 6,181,796 B1).

RE claim 1, Johnson disclose of the array driving system for driving a plurality of loads (fig.5-7; col.3 line 30-35) comprising: the plurality of loads arranged like an array (fig.5-7 wt (114,118R,118L) wt arrangement); and a plurality of driving circuits provided to correspond with the plurality of loads (fig.5-7(114R,114L); col.5 line 15-24), respectively, wherein one terminal of the plurality of loads are respectively connected to corresponding outputs of the plurality of driving circuits (fig.5-7 wt (non and inverting terminals at output at (114R,114L) ; col.5 line 20-24) and the other terminals thereof are connected each other (fig.5-7 wt (218)), and wherein driving signals are respectively supplied to the plurality of loads so that a phase of the driving signal supplied to one of the plurality of loads is opposed to that of the driving signal

Art Unit: 2615

supplied to the adjacent loads (fig.5-7 wt (120,118L,R) of different phase polarity at current entering; col.6 line 5-14) and wt inverter) and subsequent driving signals of the driving signals are generated by applying a predetermined delay to a first drive signal (fig.4, col.3 line 5-12/there is a lag/delay predetermine between the driving signals).

Re claim 2, the array driving system according to claim 1, wherein the other terminals of the plurality of loads connected each other are grounded (fig.5-7 wt (218) grounded).

Re claim 3, The array driving system according to claim 1, wherein the plurality of loads include a plurality of speaker units, the plurality of driving circuits include a plurality of amplifiers, and the plurality of speaker units are connected to the plurality of amplifiers, respectively, such that the adjacent speaker unit have an opposite polarity mutually (fig.5-7 wt (114,119) with opposite polarity).

Re claim 6, Johnson disclose of the method of driving a plurality of loads which are arranged like an array, the method comprising the steps of: respectively supplying driving signals to the plurality of loads so that a phase of the driving signal supplied to one of the plurality of loads is opposed to that of the driving signal supplied to the adjacent loads (fig.5-7 wt (120,114, -L,R) with inverting

Art Unit: 2615

opposite driving load phase), and subsequent driving signals of the driving signals are generated by applying a predetermined delay to a first drive signal (fig.4, col.3 line 5-12/there is a lag/delay predetermine between the driving signals).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable by Johnson (US 6,181,796 B1) and further in view of Official Notice.

Re claim 4, the array driving system according to claim 3, wherein an inverter are connected to the corresponding amplifiers, respectively, so as to invert phase of input signals supplied to the corresponding amplifiers (fig.5-7 wt (120); col.3 line 50). However, Johnson fail to disclose of the limitation of having the plurality of inverters. But, official notice is taken the concept of having plurality of invertors for the inputting at the amplifiers with the multiple loads is simply the designer's preference, thus it would have been obvious for one of the ordinary skill in the art to have

Art Unit: 2615

incorporated the similar concept of having numerous loads of inverting and noninverting phase with the plurality of inverters before the amplifiers for the purpose of creating opposite phase signals.

6. Claim 5 is rejected under 35 U.S.C. 102(b) as being unpatentable over Johnson (US 6,181,796 B1) and Davis (4,503,554).

Re claim 5, the array driving system according to claim 1, But, Johnson fail to disclose of the specific of having the plurality of loads include a plurality of LEDs; anodes and cathodes of adjacent LEDs are alternatively connected to a common line, ones of the plurality of driver circuits are connected between the anodes of the LEDs, cathodes of which are connected to the common line, and a positive power supply, and the others of the plurality of driver circuits are connected between the cathodes of the LEDs, anodes of which are connected to the common line, and a negative power supply. However, Davis disclose of a system with similar concept of array drivers wherein having a plurality of LEDs and anodes and cathodes of adjacent LEDs are connected to a common line, and further cathodes of which are connected to the common line, and a power supply, and anodes of which are connected to the common line, and a power supply (fig.15,17I, wt (1126,1128, with common line to interconnect and further of power supply frm resistor (1132,1102)) for the purpose of

Art Unit: 2615

indicating the working conditions of the blend circuit. Thus, taking the now combined teaching of Johnson and Davis as a whole, it would have been obvious for one of the ordinary skill in the art to have incorporated the array drivers wherein having a plurality of LEDs and anodes and cathodes of adjacent LEDs are connected to a common line, and further cathodes of which are connected to the common line, and a power supply, and anodes of which are connected to the common line, and a power supply for the purpose of indicating the working conditions of the blend circuit.

7. Claim 7 is rejected under 35 U.S.C. 102(b) as being unpatentable over Johnson (US 6,181,796 B1) and further in view of Chuang (US 6,748,096 B2).

Re claim 7, Johnson disclose of the array driving system for driving a number of loads comprising: the number of loads arranged like an array; and a number of driving circuits provided to correspond with the number of loads, respectively wherein one terminal of the number of loads are respectively connected to corresponding outputs of the n number of driving circuits and the other terminals thereof are connected each other (fig.5; col.5 line 15-24) and wherein driving signals are respectively supplied to the n number of loads so that a phase of the driving signal supplied to one of the number of loads is opposed to that of the driving signal supplied to the adjacent loads (fig.5-7 wt (120,118L,R) of different phase polarity at current entering; col.6 line 5-14) and wt inverter).

But, Johnson fail to disclose of the wiring and further the specific wherein only requires $(n+1)$ wirings for the array driving system. However, Chuang disclose of a system with wiring and further wherein the similar concept of requiring reduced wirings for the array driving system (fig.4-/ col.1 line 30-34)/reduced wiring] for the purpose of promoting aesthetic and lowering design cost. Thus, taking the combined teaching of Johnson and Chuang as a whole, it would have been obvious for one of the ordinary skill in the art at the time of the invention to have modify Johnson by incorporating the wiring and further wherein the similar concept of requiring reduced wirings (modifying the wirings to reduce such as it consist of only $(n+1)$ wirings) for the array driving system for the purpose of promoting aesthetic and lowering design cost.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Disler Paul whose telephone number is 571-270-1187. The examiner can normally be reached on 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chin Vivian can be reached on 571-272-7848. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2615

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/D. P./
Examiner, Art Unit 2615

/Vivian Chin/
Supervisory Patent Examiner, Art Unit 2615